AMENDMENTS TO THE CLAIMS

Listing of the claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

1. (Currently Amended) A CMOS sensor circuit comprising:

a photodiode;

a reset transistor resetting said photodiode to an initial voltage;

a voltage control circuit generating a reset signal in response to a reset control signal, the reset signal controlling a gate potential of said reset transistor to a potential other than power source potentials, wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first reset control signal, an N-channel MOS transistor having a gate supplied with a second reset control signal, and a transistor provided between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor to control a blooming of the CMOS sensor circuit; and

a delay circuit producing said first reset control signal which is supplied to the gate of the first P-channel MOS transistor, by delaying said second reset control signal supplied to the gate of the N-channel MOS transistor.

2. (Currently Amended) A CMOS sensor circuit comprising:

a photodiode;

a reset transistor resetting said photodiode to an initial voltage;

a voltage control circuit generating a reset signal in response to a reset control signal, the reset signal keeping a gate potential of said reset transistor from completely

becoming off, wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first reset control signal, an N-channel MOS transistor having a gate supplied with a second reset control signal, and a transistor provided between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor to control a blooming of the CMOS sensor circuit; and

a delay circuit producing said first reset control signal which is supplied to the gate of the first P-channel MOS transistor, by delaying said second reset control signal supplied to the gate of the N-channel MOS transistor.

3. (Original) The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

a transistor inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor so as to control a blooming.

4. (Original) The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

a transistor inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor so as to control a blooming.

5. (Withdrawn) The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

a transistor connected to a drain of said N-channel MOS transistor so as to control a blooming.

6. (Withdrawn) The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

a transistor connected to a drain of said N-channel MOS transistor so as to control a blooming.

7. (Withdrawn) The CMOS sensor circuit as claimed in claim 3, further comprising a plurality of serially connected transistors inserted between said drain of said first P-channel MOS transistor and said drain of said N-channel MOS transistor so as to control the blooming.

8. (Withdrawn) The CMOS sensor circuit as claimed in claim 4, further comprising a plurality of serially connected transistors inserted between said drain of said first P-channel MOS transistor and said drain of said N-channel MOS transistor so as to control the blooming.

9. (Withdrawn) The CMOS sensor circuit as claimed in claim 5, further comprising a plurality of serially connected transistors connected to said drain of said N-channel MOS transistor so as to control the blooming.

10. (Withdrawn) The CMOS sensor circuit as claimed in claim 6, further comprising a plurality of serially connected transistors connected to said drain of said N-channel MOS transistor so as to control the blooming.

11. (Original) The CMOS sensor circuit as claimed in claim 3, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor.

12. (Original) The CMOS sensor circuit as claimed in claim 4, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor.

13. (Original) The CMOS sensor circuit as claimed in claim 3, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor, and includes a gate and a drain connected to each other.

14. (Original) The CMOS sensor circuit as claimed in claim 4, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor, and includes a gate and a drain connected to each other.

15. (Withdrawn) The CMOS sensor circuit as claimed in claim 5, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor, and includes a gate and a drain connected to each other.

16. (Withdrawn) The CMOS sensor circuit as claimed in claim 6, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor, and includes a gate and a drain connected to each other.

17. (Withdrawn) The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

one of a resistance element and a diode element inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor so as to control a blooming.

18. (Withdrawn) The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

one of a resistance element and a diode element inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor so as to control a blooming.

19. (Withdrawn) The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

one of a resistance element and a diode element connected to a drain of said N-channel MOS transistor so as to control a blooming.

20. (Withdrawn) The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

one of a resistance element and a diode element connected to a drain of said N-channel MOS transistor so as to control a blooming.

21. (Withdrawn) The CMOS sensor circuit as claimed in claim 17, wherein said resistance element and said diode element are replaced by a plurality of serially connected resistance elements and a plurality of serially connected diode elements, respectively.

22. (Withdrawn) The CMOS sensor circuit as claimed in claim 18, wherein said resistance element and said diode element are replaced by a plurality of serially connected resistance elements and a plurality of serially connected diode elements, respectively.

23. (Withdrawn) The CMOS sensor circuit as claimed in claim 19, wherein said resistance element and said diode element are replaced by a plurality of serially connected resistance elements and a plurality of serially connected diode elements, respectively.

24. (Withdrawn) The CMOS sensor circuit as claimed in claim 20, wherein said resistance element and said diode element are replaced by a plurality of serially connected resistance elements and a plurality of serially connected diode elements, respectively.

Claims 25-28 (Canceled)

29. (Previously Presented) The CMOS sensor circuit as claimed in claim 1, said delay circuit is formed by an even number of inverters.

30. (Previously Presented) The CMOS sensor circuit as claimed in claim 2, said delay circuit is formed by an even number of inverters.

31. (Withdrawn) The CMOS sensor circuit as claimed in claim 3, an arbitrary bias voltage is applied to said transistor.

32. (Withdrawn) The CMOS sensor circuit as claimed in claim 4, an arbitrary bias voltage is applied to said transistor.

33. (Withdrawn) The CMOS sensor circuit as claimed in claim 5, an arbitrary bias voltage is applied to said transistor.

34. (Withdrawn) The CMOS sensor circuit as claimed in claim 6, an arbitrary bias voltage is applied to said transistor.

35. (Withdrawn) The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises an output node connected to a gate of said reset transistor, and a constant current source added to said output node.

36. (Withdrawn) The CMOS sensor circuit as claimed in claim 35, wherein said constant current source is formed by a second P-channel MOS transistor having a bias voltage applied to a gate voltage thereof.